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JUL 13 2006

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

PATENT APPLICATION:
Serial No. 10/815,521

ORIGINALLY FILED:
April 1, 2004

FOR:
VERIFICATION OF INTEGRATED CIRCUIT TESTS USING TEST SIMULATION AND INTEGRATED CIRCUIT SIMULATION WITH SIMULATED FAILURE

INVENTOR: Hildebrant, Andrew

GROUP ART UNIT: 2825

EXAMINER: Doan, Nghia M

DOCKET NUMBER: 10031350-1

ok to Enter.
08/09/2006.
NMD

SUPPLEMENTARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the phone call from the Examiner on July 13, 2006, please enter the enclosed supplemental amendment to the Supplemental Amendment filed on July 6, 2006 in the above-identified patent application and consider the remarks as follows:

Amendments to the Claims are reflected in the listing of claims which begin on page 2 of this paper.

Remarks/Arguments begin on page 10 of this paper.